WHAT IS CLAIMED IS:

1. An array substrate for an IPS-LCD device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line;

a plurality of common electrodes perpendicular to the common line, wherein the common electrodes are spaced apart from each other and at least one of the common electrodes is divided into first and second portions that are co-linear and separated by a predetermined distance; and a plurality of pixel electrodes parallel to the plurality of common electrodes, wherein the plurality of pixel and common electrodes are alternately arranged such that the array substrate is used for the IPS-LCD device.

2. The array substrate of claim 1, wherein the first and second portions of the common electrode are about equal in length such that first and second domains for a liquid crystal are produced by the array substrate.

3. The array substrate of claim 1, wherein the pixel electrode adjacent the first and second portions of the common electrode includes a male electrode opposing a boundary between the first and second portions of the common electrode.

4. The array substrate of claim 1, wherein at least one of the pixel electrodes is divided into first and second portions that are coaxial.

5. The array substrate of claim 4, wherein the second portions of the common and pixel electrodes are about twice as long as the first portions of, respectively, the common and pixel electrodes, the first portion of the common electrode opposes the second portion of the pixel

electrode, and the second portion of the common electrode opposes the first portion of the pixel electrode.

6. The array substrate of claim 5, wherein the common electrode adjacent the pixel electrode includes a male electrode that opposes a boundary between the first and second portions of the pixel electrode.

7. The array substrate of claim 5, wherein the pixel electrode adjacent the common electrode includes a male electrode that opposes a boundary between the first and second portions of the common electrode.

8. The array substrate of claim 1, wherein the pixel electrode is selected from a group consisting of indium tin oxide (ITO) and indium zinc oxide (IZO).

9. The array substrate of claim 1, wherein the common electrode is selected from a group consisting of chromium (Cr), aluminum (Al), aluminum alloy (Al alloy), molybdenum (Mo), tantalum (Ta), tungsten (W), antimony (Sb), and an alloy thereof.

10. The array substrate of claim 1, wherein the common electrode is selected from a group consisting of indium tin oxide (ITO) and indium zinc oxide (IZO).

11. An array substrate for an IPS-LCD device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a main common line parallel to the gate line;

first and second auxiliary common lines perpendicular to the main common line, the first and second auxiliary common lines being parallel to and spaced apart from each other;

a plurality of common electrodes perpendicular to the first and second auxiliary common lines, the common electrodes being spaced apart from each other and at least one of the common electrodes divided into first and second portions that are co-linear and separated by a predetermined distance; and

a plurality of pixel electrodes parallel to the plurality of common electrodes, wherein the plurality of pixel and common electrodes are alternately arranged.

12. The array substrate of claim 11, wherein the first and second portions are about equal in length such that first and second domains for a liquid crystal are produced by the array substrate.

13. The array substrate of claim 11, wherein the pixel electrode adjacent the first and second portions of the common electrode includes a male electrode that opposes a boundary between the first and second portions.

14. The array substrate of claim 11, wherein at least one of the pixel electrodes is divided into first and second portions that are co-linear and separated by a predetermined distance.

15. The array substrate of claim 14, wherein the second portions of the common and pixel electrodes are about twice as long as the first portions of, respectively, the common and pixel electrodes, wherein at least one of the first portions of the common electrodes opposes at least one of the second portions of the pixel electrodes, and at least one of the second portions of the common electrodes opposes at least one of the first portions of the pixel electrodes.

16. The array substrate of claim 11, wherein the common electrode adjacent the pixel electrode includes a male electrode adjacent to a boundary region between the first and second portions of the pixel electrode.

17. The array substrate of claim 14, wherein the pixel electrode adjacent the common electrode includes a male electrode adjacent to a boundary between the first and second portions of the common electrode.

18. An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line;

a plurality of common electrodes extending perpendicular to the common line;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes;

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel electrodes is spaced apart from the auxiliary common electrode; and pixel electrodes are on a same layer.

19. An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line, the common line including first and second auxiliary common lines perpendicular to the common line;

a plurality of common electrodes extending perpendicular to the first and second auxiliary common lines;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes;

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes, wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.

20. An array substrate for an IPS-LCD device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a common line parallel to the gate line, the common line including a plurality of common electrodes extending perpendicular to the common line;

a plurality of pixel electrodes arranged alternately with the plurality of common electrodes; and

a plurality of auxiliary electrodes connecting the plurality of common and pixel electrodes in a check pattern.

21. An array substrate for an IPS-LCD device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a pixel region surrounded by the gate and data lines, the pixel region including first and second domains;

a transparent pixel electrode including:

first and second perpendicular pixel electrodes,

a plurality of first transverse pixel electrodes, and

a second transverse pixel electrode, wherein the first perpendicular pixel electrode is disposed along the first and second domains and is perpendicular to the gate line, wherein the second perpendicular pixel electrode is disposed on the second domain and parallel to the first perpendicular pixel electrode, wherein the plurality of first transverse pixel electrodes perpendicularly extends from the first perpendicular pixel electrode on the first domain, and wherein the second transverse pixel electrode connects the first and second perpendicular pixel electrodes on the second domain;

a common line parallel to the gate line; and

a common electrode including:

(a) first to third perpendicular common electrodes,

(b) a plurality of first transverse common electrodes, and

(c) a second transverse common electrode, wherein the first and second perpendicular common electrode is disposed along the first and second domains and is parallel to the first and second perpendicular pixel electrodes, wherein the third perpendicular common electrode is disposed on the second domain between the first and second perpendicular common electrodes, wherein the plurality of first transverse common electrodes are alternately arranged with the plurality of transverse pixel electrodes on the first domain, and wherein the second transverse common electrode connects the first to third perpendicular common electrodes.

22. The array substrate of claim 21, wherein an outermost first transverse pixel electrode overlaps a portion of the gate line.

23. The array substrate of claim 21, wherein the common electrode is a transparent conductive material.

24. The array substrate of claim 21, further comprising an alignment layer having first and second rubbing directions, which correspond to the first and second domains, respectively.

25. A method for fabricating an array substrate of an IPS-LCD device, the method comprising:

preparing a substrate;

forming a gate line including a gate electrode on the substrate;

forming a gate-insulating layer on the substrate such that the gate-insulating layer covers the gate line and gate electrode;

forming an active layer and ohmic contact layer on the gate-insulating layer;

forming a data line including a source electrode, and a drain electrode on the gate-insulating layer;

forming a first passivation layer on the gate-insulating layer such that the first passivation layer covers the data line, source electrode, and drain electrode, the gate-insulating layer having a drain contact hole over the drain electrode;

forming a pixel electrode on the first passivation layer, the pixel electrode including first and second perpendicular pixel electrodes, a plurality of first transverse pixel electrodes, and a second transverse pixel electrode, wherein the first perpendicular pixel electrode is disposed along the first and second domains and perpendicular to the gate line, the second perpendicular pixel electrode is disposed on the second domain and parallel to the first perpendicular pixel electrode, the plurality of first transverse pixel electrodes perpendicularly extends from the first perpendicular pixel electrode on the first domain, and the second transverse pixel electrode connects the first and second perpendicular pixel electrodes on the second domain;

forming a second passivation layer on the pixel electrode;

forming a common line including a common electrode on the second passivation layer, the common electrode including first to third perpendicular common electrodes, a plurality of first transverse common electrodes, and a second transverse common electrode, wherein the first and second perpendicular common electrodes are disposed along the first and second domains and are parallel to the first and second perpendicular pixel electrodes, wherein the third perpendicular common electrode is disposed on the second domain and between the first and second perpendicular common electrodes, wherein the plurality of first transverse common electrodes are alternately arranged with the plurality of transverse pixel electrodes on the first domain, and wherein the second transverse common electrode connects the first to third perpendicular common electrodes; and

forming an alignment layer on the common electrode, the alignment layer having first and second rubbing directions.

26. The method of claim 25, further comprising the step of forming a planar layer on the common electrode before forming the alignment layer.

27. The array substrate of claim 25, wherein an outermost first transverse pixel electrode overlaps a portion of the gate line.

28. The array substrate of claim 25, wherein the common electrode is a transparent conductive material.

29. The method of claim 25, wherein the first and second rubbing directions are symmetrical with respect to a line parallel to the gate line.

30. An array substrate for an LCD-device, the array substrate comprising:

a substrate;

a gate line on the substrate;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a pixel region surrounded by the gate and data lines, the pixel region including first and second domains;

transverse pixel and common electrodes disposed on the first domain and parallel to the gate line, the transverse pixel and common electrodes being alternately arranged;

perpendicular pixel and common electrodes disposed on the second domain and perpendicular to the transverse pixel and common electrodes, respectively, the perpendicular pixel and common electrodes being alternately arranged; and

an alignment layer having first and second rubbing directions, the first and second rubbing directions corresponding to the first and second domains, respectively.

31. The array substrate of claim 16, wherein the male electrode connects the first and second portions of the common electrode.

32. The array substrate of claim 17, wherein the male electrode connects the first and second portions of the pixel electrode.

33. An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a gate insulating layer over the gate line;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a first passivation layer over the gate insulating layer, the data line and thin film transistor;

a plurality of pixel electrodes on the first passivation layer;

a second passivation layer over the pixel electrodes;

a common line on the second passivation layer and parallel to the gate line, the common line including first and second auxiliary common lines perpendicular to the common line;

a plurality of common electrodes extending perpendicular to the first and second auxiliary common lines;

an auxiliary common electrode perpendicularly contacting each common electrode; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode; and

wherein the pixel electrodes are arranged alternately with the common electrodes.

34. An array substrate for an IPS-LCD device, comprising:

a substrate;

a gate line on the substrate;

a gate insulating layer on the gate line;

a data line perpendicular to the gate line;

a thin film transistor at a crossing portion between the gate and data lines;

a first passivation layer over the gate insulating layer, the data line and the thin film transistor;

a plurality of pixel electrodes on the first passivation layer;

a second passivation layer over the pixel electrodes;

a common line on the second pass layer parallel to the gate line;

a plurality of common electrodes on the second passivation layer perpendicular to the common line and arranged alternatively with the pixel electrodes;

a plurality of common electrodes on the second passivation layer perpendicular to the common line and arranged alternatively with the pixel electrodes;

an auxiliary common electrode perpendicularly contacting each of the common electrodes; and

an auxiliary pixel electrode perpendicularly contacting each of the pixel electrodes;

wherein the auxiliary pixel electrode is spaced apart from the auxiliary common electrode.